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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,235	06/19/2003	Gary K. Richmond	7281-US	9810

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EXAMINER	
DESTA, ELIAS	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,235	RICHMOND, GARY K.	
	Examiner	Art Unit	
	Elias Desta	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/13/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-17* is/are rejected.

7)☒ Claim(s) *11 and 18-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *06/13/2003* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Abstract

1. Applicant is reminded of the proper content of an abstract of the disclosure; in the instant application, the abstract is too short in explaining the technical disclosure of the improvement.

Claim Objection

2. Claim 3 is objected to because of the following minor informalities:

- Page 19, line 16, insert "are" after transitions.

Claim rejection – 35 U.S.C. 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. *Claims 1-10 and 12-17* are rejected under 35 U.S.C. 102(b) as anticipated by *Hall, Jr.* (U.S. Patent 4,349,896).

In reference to claims 1 and 10: *Hall, Jr.* teaches an apparatus that includes:

- An analog sampling array (see *Hall, Jr.*, Fig. 2, signals from receivers 24's), for acquiring from the signal under test (SUT) (or acoustic signals from the wheels) a plurality of temporally offset analog samples during each of the sequence of sample periods (see signals from the receiver in Fig. 2 and Fig. 3, from the output);
- A plurality of sample processors (see *Hall, Jr.*, Figs. 4-5), for identifying logic level transactions between respective current and previous samples and for determining a time of occurrence of the logic level transaction (see *Hall, Jr.*, column 4, lines 44-63); and

Further, *Hall, Jr.* also includes a method for

- Determining a logic level for each of the analog samples using a threshold signal level (see *Hall, Jr.*, Figs. 2 and 3);
- Generate edge bin data structure (see *Hall, Jr.*, Fig. 5, output from member 42 or the peak detector); and
- Edge bin data structure includes identification of a sample associated with logic level transition and estimation of the relative threshold level crossing time of the signal under test (SUT) between successive sample (see *Hall, Jr.*, Fig. 2, transmitter burst with suppressed noise in between successive signals, such as shear wave).

With regard to claim 2: as noted above in claim 1, *Hall, Jr.* further teaches that the apparatus includes a time stamp processor, for imparting a time stamp to sample data indicative of respective sample times (see *Hall, Jr.*, column 5, line 64 to column 6, line 8).

With regard to claim 3: as noted above in claim 1, *Hall, Jr.* further teaches that the samples are acquired and logic level transitions are identified in real time (see *Hall, Jr.*, column 4, lines 44-51).

With regard to claim 4: as noted above in claim 1, *Hall, Jr.* further teaches that the sample intervals are defined as respective temporal portions of a period of a clock (see *Hall, Jr.*, column 4, line 64 to column 5, line 26).

With regard to claim 5: as noted above in claim 1, *Hall, Jr.* further teaches that the plurality of processors shown in Fig. 5 include a convolution and pick detector, hence it is inherent for each sample period, each the sample processor receives respective current sample (Vc) and respective previous sample (Vp) and responsively produces sample data including indication of logic level of the current sample (L), such as identifying logic level transition between the current and previous samples (E) and estimated time of occurrence of the identified logic level transition.

With regard to claims 6 and 11: as noted above in claim 5, *Hall, Jr.* further teaches that the apparatus includes reduction logic (see *Hall, Jr.*, Fig. 2, removing inherent system noise using thresholds and amplitude detection), for reducing the

amount data provided to the time stamp processor by discarding (removing the noise component, see *Hall, Jr.*, column 4, lines 19-37) sample data not associated with an identified logic level transition.

With regard to claim 7: as noted in claim 6, *Hall, Jr.* further teaches that the sample data produced by each sample processors (see Fig. 5, Expanded output) is associated with a respective slice identifier (see *Hall, Jr.*, Fig. 5, peak detector).

With regard to claim 9: as noted above in claim 1, *Hall, Jr.* further teaches that the sample data where the system includes a plurality of instances of the apparatus are used to process respective signals under test including a clock signal and a data signal (see *Hall, Jr.*, Fig. 5, member 44, signal from pick detector and clock signal to 44).

With regard to claim 12: as noted above in claim 10, *Hall, Jr.* further teaches that the signal under test (SUT) includes a data signal, and the edge bin data (see Fig. 5, data from pick detector) structure, which includes logic level indicator [see *Hall, Jr.*, Fig. 5, the output from "compression wave storage" or member 44, since all the input member 30 (sample & hold) or member 44 provide a logic level indicator for the purposes of conversion form analog to digital signal].

With regard to claim 13: as noted above in claim 10, *Hall, Jr.* further teaches that the edge bin structure (pick detector) includes a time stamp indicative of the time of a respective threshold level transition of the signal under test (SUT) (input

signal from the receiver as shown in Figs. 4 and 5; output that is delayed or time expanded output).

With regard to claims 14 and 17: as noted above in claim 10, *Hall, Jr.* further teaches that the method is used to process each of a plurality of signals under test including clock signal and a data signal to produce corresponding list of edge bins (edge detected signals (see *Hall, Jr.*, Fig. 5, output from member 42); and processing each data signal edge list with the clock signal edge bin list (since clock signals are triggered at some transition time) to identify, for each clock signal edge, corresponding logic value of the data signal (the expanded output from member 44 of Fig. 5).

With regard to claims 15 and 16: as noted above in claim 14, *Hall, Jr.* further teaches that the method of processing each data signal edge bin list (pick detected) with the clock signal edge bin (clock) list to identify a timing violation because in sampling and holding, it is inherent that a rule has to have a way to detecting a violation since convolution operation or an A/D conversion would not have been possible under the circumstances (as shown in Fig. 5).

Allowable Subject Matter

5. *Claims 11 and 18-21* are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant disclosure:

- *Doggett* (U.S. Patent 4,598,398) teaches test apparatus for PCM/FDM trans-multiplexer.
- *Gribbes et al.* (U.S. Patent 4,204,433) teaches computerized ultrasonic scanner with technique select.
- *Bauernfeind et al.* (U.S. Patent 4,302,843) teaches method and apparatus for measuring transmission characteristics of test object during communication gap.
- *Payton et al.* (U.S. Patent 4,168,485) teaches simultaneous use of pseudo-random control signals in vibration exploration method.
- *Meditch et al.* (IRE Publication, 'On the Real-Time Control of Time-Varying Linear System') teaches a new class of sampled data controls for time varying dynamic process.

- *Lewes* (IEEE Article, 'Optimizing the Stage Resolution in Pipelined, Multistage, Analog-to-Digital Converters for Video-Rate Applications') teaches the effect of stage resolution on the characteristics of monolithic, pipelined, multi-state, analog-to-digital converters (ADCs).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Desta whose telephone number is (703)-305-3840. The examiner can normally be reached on M-Thu (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)-308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-5841 for regular communications and (703)-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-1782.

Elias Desta
Examiner
Art Unit 2857

-ed

January 15, 2004

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800